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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/016,008      | 12/11/2001  | Takehito Ushiki      |                     | 3846             |

26021 7590 05/19/2003

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EXAMINER

DEO, DUY VU NGUYEN

|          |              |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

1765

DATE MAILED: 05/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/016,008

Applicant(s)

USHIKI ET AL.

Examiner

DuyVu n Deo

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1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 14-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 09/346,004.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kato et al. (US 5,447,890).

Kato describes a method for producing a wafer comprising polishing a surface of the semiconductor wafer to get a mirror finish (col. 4, line 43-54; col. 5, line 17-24). This mirror polishing is well known to one skill in the art to include holding the wafer at its back and polishing the other surface (please see background art in page 2 of the specification). Column 4, line 65-col. 5, line 5, line 17-24, in Kato describe the reversed surface (claimed back surface) after the treatment and before polish the observed surface (or claimed before holding the wafer for the polishing of the observed surface) with a roughness having an amply shorter period than the undulation W1 (in the approximate range of 1-10 um) and a P-V value in the approximate

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range of 0.1-0.5  $\mu\text{m}$  is formed on the reversed surface (or back side). This shows the back surface profile and its frequency have to be determined or analyzed, before polishing the observed surface, to have above data about the reversed surface (or claimed back surface).

Although Kato does not explicitly teach the limitations of the wafer having undulation components on wafer back surface of 10  $\mu\text{m}^3$  or less represented in terms of power spectrum density at least for the components at a wavelength of 10 mm and/or a variation of power spectrum density of 2.0 or less for undulation components at a wavelength of from 3mm to 20 mm of the wafer back surface, it is reasonable to presume that said limitations are inherent to the invention. Support for said presumption is found in the use of similar materials (i.e. silicon wafer: col. 1, line 5-10), an undulation of 1-10  $\mu\text{m}$ : col. 5, line 3 (this reads on claim 15 of wafer warpage of 20  $\mu\text{m}$  or less) and in the similar production steps (i.e. alkali etching: col. 6, line 31-34; and polishing to a mirror finish) used to produce the semiconductor wafer. The burden is upon the Applicant to prove otherwise. *In re Fitzgerald*, 205 USPQ 594. In the alternative, the claimed power spectrum density, variation of power spectrum density would obviously have been provided by the process disclosed by Kato. Note in *re Best*, 195 USPQ 433, footnote 4 (CCPA 1977) as to the providing of this rejection under 35 USC 103 in addition to the rejection made above under 35 USC 102.

Further, in the alternative, Kato's method describes the reversed surface-polishing step in order to remove undulations, or irregularities according to page 3 of specification, on the reversed side of the wafer (col. 2, line 45-51) before the polishing of the observed surface as described above. It would be obviously to one skill in the art by Kato's teaching that it is desired to have less irregularity in the back surface. Therefore, his method can be used to polish a wafer

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that less irregularity the better, including wafer having claimed irregularity of having undulation components on wafer back surface of 10  $\mu\text{m}^3$  or less represented in terms of power spectrum density at least for the components at a wavelength of 10 mm and/or a variation of power spectrum density of 2.0 or less for undulation components at a wavelength of from 3mm to 20 mm in order to produce a mirror surface with a reasonable expectation of success.

Referring to claim 15, the an undulation of 1-10  $\mu\text{m}$  described in col. 5, line 3 reads on wafer warpage of 20  $\mu\text{m}$  or less.

Referring to claims 16, 17, the wafer is silicon semiconductor wafer (col. 1, line 5-10).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 703-305-0515.

DVD

May 15, 2003

